REMARKS

The Office Action of February 24, 2004 was received and carefully reviewed. Reconsideration and withdrawal of the currently pending rejections are requested for the reasons advanced in detail below.

Claims 1-6 and 15-28 were pending prior to the instant amendment. By this amendment, claims 1, 3, 5, 15, 20, 23 and 27 are amended. Consequently, claims 1-6 and 15-28 remain currently pending in the instant application.

Initially, Applicant acknowledges with appreciation the courtesies extended during the Examiner's interview of April 14, 2004.

Addressing the Office Action, claims 1, 3, 5 and 15 are objected to because of informalities. In response thereto, claims 1, 3, 5 and 15 are amended herein at line 3 to replace "minor" with –mirror--.

Claims 1-6, 15, 16, 19, 20, 22, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's prior art as shown in instant figure 5 in view of U.S. 5,365,875 to Asai et al. (of record); and claims 17, 18, 21, 23, 24, 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's prior art in view of Asai et al. and further in view of Dabral et al. (of record). These rejections are traversed for the reasons advanced in detail below.

In order to operate a buffer circuit, it is helpful to include two mirror circuits. Due to differences in crystallization, however, the current generated can be very different causing offset voltage. As a result, suppression of the characteristic variation in mirror circuits is important. In the present invention, the semiconductor device includes an analog buffer including first and second transistors wherein a gate length of the first and second thin film transistors is twice or more as compared with the gate length of a third transistor. This feature is recited in claims 1, 3, 5, 15 and 20 and is supported in the specification by Figure 8 and lines 4-7 of page 16. This feature is not disclosed or suggested in Applicant's prior art or Asai et al. As a result, Applicant respectfully requests that the rejection of claims 1, 3, 5, 15 and 20, as well as the claims depending therefrom, be reconsidered and withdrawn.

With respect to the rejection of claim 25, this claim recites criss-cross design, namely, semiconductor device including an analog bugger wherein a first and a second thin film transistor are connected in parallel with each other and located in a cross arrangement. This

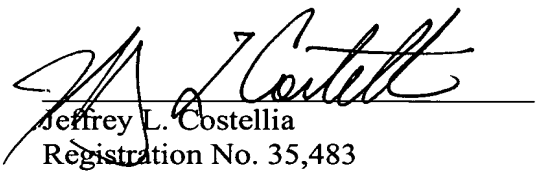
feature is clearly disclosed in Figure 11A, as discussed during the Examiner's interview. Applicant's prior art nor Asai et al., either alone or in combination, teach or suggest this feature. Therefore, claim 25, as well as claim 26 depending therefrom, should be considered allowable.

Claims 17, 18, 21, 23 24, 27 and 28 are rejected under 35 U.S.C. 103(a) over Applicant's prior art and Asai et al., and further in view of Dabral et al. This rejection is traversed for the reasons advanced below.

Claims 23 and 27 are amended to recite the above discussed feature that the gate length of the first and second thin film transistors is twice or more as compared with the gate length of a third thin film transistor. This feature is not disclosed in Applicant's prior art, Asai et al., or Dabral et al., either alone or in combination with each other. As a result, this rejection should also be reconsidered and withdrawn.

In view of the foregoing, it is respectfully requested that the rejections of record be reconsidered and withdrawn by the Examiner, that claims 1-6 and 15-28 be allowed and that the application be passed to issue. If a conference would expedite prosecution of the instant application, the Examiner is hereby invited to telephone the undersigned to arrange such a conference.

Respectfully submitted,



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